Electrical properties of Graphene/Silicon structure with Al₂O₃ interlayer

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Abstract



1 Introduction

Graphene (Gr) has attracted the attention of many researchers, thanks to its excellent electrical [1–6], mechanical [7], optical [8], and thermal properties [9]. Graphene is one of the most significant among all two-dimensional (2D) materials due to its important properties such as high thermal conductivity, high transparency, high electrical conductivity, high carrier mobility, low contact resistance, and mechanical flexibility [10]. Graphene is an impressive material for future electronics due to these properties and is used in various electronic and photonic devices such as transistors, electrodes, gas sensors, photodetectors, solar cells, microwave mixers, rectifiers, graphene variable-barrier "barristor", and some integrated circuits [2–4]. These graphene with

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semiconductor technology. For example, the graphene/silicon (Gr/Si) junction is one of the simplest devices.

In the literature, various methods such as CVD, pulsed laser deposition (PLD), plasma-enhanced chemical vapor deposition (PECVD), and epitaxial growth have been used to grow Graphene and Graphene-based nanostructures. There is no standard method for the fabrication of the Gr/ Si structure. Each method involves different parameters in itself. Especially some parameters such as growth of Graphene, transfer process of Graphene, the effects of substrate and oxide layer, the geometry of the substrate, the effect of metal-Graphene contact should be reviewed together. Despite the excitement of both experimental and theoretical studies, the physics underlying the Graphene-semiconductor structure is unfinished yet [2, 4].

Up to now, some researchers examined Graphene-based Schottky structures [2–4, 11]. The source of the non-ideal Graphene-Silicon Schottky junction was examined by Zhang et al. [12]. They found that native oxide (SiO_2) is proved to be an important role in finding the behavior of a Gr-Si junction. Tomer et al. [13] fabricated Schottky junctions by CVD monolayer Gr on *n*-Si and GaAs wafers and investigated inhomogeneity in barrier height Gr/Si (or GaAs) structures. Luongo et al. [14] studied the importance of the wafer in Gr/Si photodiodes. They concluded that the substrate tip geometry effects Gr/p-Si Schottky



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diode performance. The influence of temperature and light on the I-V/C-V properties of Gr/n-Si. Schottky diodes were characterized by Luongo et al. [15]. They notified a very high photocurrent and concluded that the structure enhances the photo-response of Gr/Si junction.

Herein we experimentally investigate the effect of inserting a high dielectric layer as (Aluminium oxide- Al_2O_3) between the Gr and Si. The layer acts as an electron blocking layer and the affective modulation of the Graphene's Fermi level to passivate the silicon surface, which not only minimizes recombination but also increases the built-in potential. Therefore, Al₂O₃ was used as a high dielectric layer between the Gr and Si. The benefits of Al₂O₃ interfacial layers are not only limited to reducing the recombination at the interface but it also creates a higher Schottky barrier. Al₂O₃ has been proven as a good passivation layer for Si substrate [16, 17]. Passivating the surface with Al₂O₃ prevents thick native oxide formation at the interface. Also, it creates a conformal and uniform Al₂O₃ layer passivating the Si surface effectively. Thus, the Al₂O₃ layer contributed to improving the carrier lifetime for Si substrate decreasing the series resistance, reducing the surface recombination, and decreasing the density of traps significantly causing a major reduction in the surface recombination. Consequently, the Al_2O_3 interlayer between Gr and Si plays an important role in improving C-V and G-V characteristics of the Al₂O₃ layer between the Gr and Si.

The interface state density (D_{it}) and series resistance (R_s) are important parameters affecting the electrical characteristics of semiconductor devices [18, 19]. The current-voltage (I-V), capacitance-voltage (C-V), and conductance method are used to determine the D_{it} and R_s parameters. The D_{it} and R_s are strongly dependent on alternating current frequency. Therefore, the C-V and G-V characteristics are sensitive to applied voltage and the frequency. The interface states cause the C-V curves to be stretched out along the gate voltage axis. The interface states cause the nonparallel shift or stretch out along the gate voltage axis of the C-V curves.

In this research article, we investigated the frequencysensitive capacitance/conductance-voltage (C/G-V) characteristics of the Al/Gr/Al₂O₃/p-Si structure. The admittance measurements ($Y = G + i\omega C$) were performed in the frequency range of 10 kHz–400 kHz and at 300 K. The voltage limit was adjusted to $\pm 5V$ dc. The electrical parameters such as interface states and series resistance of the structure were extracted from the admittance measurements. Aluminum oxide (Al₂O₃) thin films were deposited at room temperature onto the p-Si wafer by Radio Frequency (RF) magnetron sputtering. The CVD method, which is the standard method [3] was applied for the deposition of monolayer graphene onto Al₂O₃/p-type Si.

2 Experimental details

In this study, firstly, Graphene nanosheets were deposited on the copper (Cu) (99.99% purity from Alpha Easer) substrates by using the CVD procedure. The procedure is widely used to obtain homogenous and single-layer Graphene nanosheets compared to other techniques. CH₄ gas as the carbon source, H_2 gas for both the diluent gas and the annealing process gas, and Ar and H₂ gases were used together to facilitate the breakdown CH₄ precursor. First of all, the Cu substrates were cut to size $2 \text{ cm} \times 2 \text{ cm}$, and no surface cleaning was performed for these substrates. These Cu substrates were placed in the substrate compartment of the CVD technique and the pressure of the vacuum medium was set to 1 mTorr with the help of the vacuum pump. At this pressure, annealing of these metal substrates was carried out. First, the temperature of the vacuum medium was removed from 24 °C to 1000 °C by 40 minutes using the heater. The process was executed by using 20 sccm H₂ gas and 15 sccm Ar gas for 30 minutes at 1000 °C. The Gr thin films were then obtained by sending 7 sccm CH₄ gas to the vacuum medium without changing the gas flow rates of these gases for 30 minutes. Growth details of Gr nanosheets are presented in Fig. 1 [15]. After the growth procedure, the Gr nanosheets were moved onto the above-mentioned (Al₂O₃)/p-Si structure. After the growth procedure, the Gr transfer process on to Al₂O₃/p-Si structure was occurred using with standard approach Poly(methyl methacrylate (PMMA)/Iron(III) Chloride (FeCl₃) as seen in Fig. 2 [16].

The numbers of CVD graphene layers were determined by using Raman analysis. Raman analysis provides detailed information to investigate the characteristic peaks of carbonbased films and to determine the number of layers by calculating the ratios of these peaks relative to each other. However, optical transmittance analysis and TEM analysis are also preferred for the detection of Graphene layer numbers



Fig. 1 Graphene growth mechanism on Cu foil by the CVD method



Fig. 2 The schematic illustration of the Graphene transfer process

or to support each other. The optical transmittance is generally known as 97.6% for single-layer graphene, and with each increasing number of layers, this ratio decreases to 2.4. On the other hand, TEM analysis, besides determining the number of layers, is the most obvious method used to identify wrinkles, that is, defects caused by possible etching resiudes used in the Graphene transfer process. In this study, Raman analysis was preferred for the determination of the number of layers. In addition to determining the number of layers, TEM analysis was additionally performed to see the negative effects of the transfer process. Determination of the number of layers of CVD Gr films was carried out by Raman spectra as seen in Fig. 3. This figure presents the G and 2D characteristic peaks at 1587 cm⁻¹ and 2691 cm⁻¹, respectively. Also, some peaks such as D and D+G have been identified, but these peaks are very weak. The presence of D, G, and 2D peaks in Raman spectrum and the ratios of their intensity relative to each other play a very important role in determining the number of Graphene layers obtained. The ratio of I_{2D}/I_G peak intensities is often used by many researchers to determine the number of layers. In the literature, some important information such as defect and number of layers can be provided by determining the ratios of other characteristic peaks, but the most common



 $\ensuremath{\mbox{Fig. 3}}$ Determination of the number of graphene layers by using Raman spectra

approach for CVD Graphene is the I_{2D}/I_G ratio [20, 21]. Here, if this ratio is > 2, it is called monolayer and < 2 if several [22, 23]. These I_{2D}/I_G ratios of Gr films obtained by CVD technique were calculated as 2.27, 2.01, and 1.78, respectively, and these films were coded as MLG1, MLG2, and MLG3, respectively. However, the MLG3 sample can also be called partially 1–2 layers, that is, it can also be defined as a bilayer. TEM analysis was carried out to see the negative effects of the transfer of CVD Graphene and to confirm the number of layers detected by Raman analysis and is presented in Fig. 4 [24]. This graph shows that the CVD graph covers perfectly on the p-Si used as a substrate, that is, there is no wrinkle, and it is also monolayer. This analysis was performed only for MLG1.



Fig. 4 TEM image for MLG1

124 nm thick Aluminum (Al) (pureness: 99.99%) for an ohmic contact was coated by using the thermal evaporation (TE) technique. To dope Al into the unpolished surface of the p-type Si (100), the p-Si (having resistivity of 1–10 Ω cm, the diameter of 2 inches, and thickness of 280 µm) was annealed at 500 °C/10 min in vacuum by TE technique. Later, Al₂O₃ thin films were deposited at room temperature onto p-Si by RF magnetron sputtering. For this, an Al₂O₃ target of 99.9% purity was used. The power was 150 W and the base pressure inside the chamber was always 3.3×10^{-7} mbar. The coating pressure was $4.2.10^{-3}$ mbar. The target to substrate distance was fixed at 50 mm to achieve a better homogeneity. The working gas was 99.99% Ar. Ar/ O_2 gas flow ratio was 9/1 and Ar flow rate was 12 sccm, O_2 flow rate was 1.3 sccm. The deposition rate is 0.1 Å/s. The thickness of Al₂O₃ was 17 nm. The Al₂O₃/p-Si structure was immersed in deionized water so that the Gr thin film was placed on this structure. In the final step, the thickness of 128 nm Al metal for rectifying contacts was deposited using by TE technique on Gr nanosheet by a 1 mm diameter metal mask. Figure 5 shows the schematic profile of the prepared Al/Gr/Al₂O₃/p-Si structure.

3 Results and discussion

Graphene is transparent in this Gr/Al₂O₃/p-Si structure and Gr transparent electrodes are used as an essential part of electronic and optoelectronic devices. Any work function difference between the Gr and the metal electrode will result in charge transfer, which creates an electrostatic barrier in the form of a dipole layer at the Gr/electrode interface. The energy band diagram of the Gr/Al₂O₃/p-Si structure is shown in Fig. 6 where insulator (high- κ) layer, $\varphi_{\rm bm}$ and $\varphi_{\rm T}$ are defined as Al₂O₃ layer, the effective barrier height, the effective barrier height of the insulator layer, respectively. In this structure, carrier transport is assumed to conform to a thermionic emission mechanism as occurring in a conventional metal-semiconductor (MS) connection.

In the present study, frequency-dependent G-V/C-V results of Al/Gr/Al₂O₃/p-Si structure had been studied at 10 kHz-400 kHz. Besides, the voltage limit was measured



Fig. 5 The schematic profile of the prepared Al/Gr/Al_2O_3/p-Si structure



Fig. 6 The energy band diagram of the Al/Gr/Al₂O₃/p-Si structure

from $\pm 5V$ dc. C - V/G - V plots of the prepared structure are shown in Figs. 7 and 8, respectively. C-V graphs indicate p-type wafer doings for each frequency. The capacitance values decrease with the increase in frequency. The capacitance depends on the frequency of the applied alternating current (ac) signal. This behavior is relating to the presence of interface states at the Al₂O₃/p-Si interface. Under high frequency condition, the charges at the interface states have a lifetime (τ) larger than 1/ ω (ω is angular frequency). Therefore, they can't follow up on the aac signal [16, 17]. In this case, interface states are in equilibrium with the semiconductor. There is an unimportant contribution at capacitance due to the interface states. Moreover, the charge carriers can be trapped in the Gr/Al₂O₃ interface. If the applied ac frequency is low, the minority carriers can follow the ac signal. In this case, the interface states contribute to the capacitance. Conductance and capacitance values depend on several parameters such as energy distribution and series resistance, interface states or formation, and thickness of



Fig. 7 Capacitance–voltage (C–V) plots of the Al/Gr/Al₂O₃/p-Si structure in the frequency range of 10 kHz to 400 kHz



Fig.8 Conductance–voltage (G-V) plots of the Al/Gr/Al2O3/p-Si structure

 Al_2O_3 and Gr. Therefore, a higher C value is observed at low frequencies. Because the interface layer with Gr/Al_2O_3 changes the number of interface charges and this causes a change in the depletion layer of structure with Gr/Al_2O_3 . The capacitance of such an inhomogeneous charge layer at the semiconductor/interface layer will contribute an additional capacitance with the interface layer capacitance causing frequency dispersion.

Therefore the total capacity of Al/Gr/Al₂O₃/p-Si structure with accumulation, depletion, and inversion region as the sum of the silicon capacitance, interface traps capacitance the insulator capacitance is and given $1/C = 1/C_{ins} + 1/(C_s + C_{it})$. While the interface traps yield an excess frequency-dependent capacitance (C_{it}) and respond to ac voltage change at lower frequencies. The contribution of interface trap capacitance is negligibly small at high frequencies region. The total capacitance value is maximum at the accumulation region and $C = C_{ins}$. For the depletion region, as the silicon capacitance increases by the formation of the depletion layer, the total capacitance decreases as they are in series with each other. Finally, for the inversion region, total capacitance is the series combination of insulator capacitance and inversion layer capacitance. Also, the C-Vgraphs give a peak in the depletion region. This is because interface states placed in the forbidden energy gap, existing of series resistance, doping concentration, and thickness of the interfacial insulator layer [18, 25–36]. Interface states are impressive in the depletion and inversion regions. As seen in Fig. 7, in contrast to C values, the measured G values increase with increasing frequency. Conductance (G = 1/R)is related to the R_s . The increase of G is due to the decrease of $R_{\rm s}$ with increasing frequency.

Usually, series resistance (R_s) in the semiconductor devices corresponds to the contact resistances of the metal

Fig. 9 Series resistance–voltage (R_s-V) plots of the structure

-2

3.0x10

2.5x10

2.0x10

1.5x10

 1.0×10^{3}

5.0x10

-6

 $\mathbf{R}_{\mathbf{s}}(\Omega)$

electrodes. For this reason, it is an important parameter that cause a change in electrical features. To calculate the series resistance, the following relation is given as [25-36]:

V (V)

$$R_{\rm s} = \frac{G_{\rm m}}{G_{\rm m}^2 + \omega^2 C_{\rm m}^2} \tag{1}$$

where $G_{\rm m}$ (measured-conductance) and $C_{\rm m}$ (measuredcapacitance) in the accumulation zone respectively. For different frequencies, R_s -V graphs are presented in Fig. 9. It is seen that the R_s weren't dependent on the voltage at the positive bias and accumulation zone. Also, the $R_{\rm s}$ values increase with decreasing frequency due to the interface charges dependent on the frequency. In obtaining frequency and voltage-dependent characteristics of the structure, R_s must be taken into consideration. Besides, R_s -V curves show a peak. The peak size increases with reducing the frequency and the position of peak shifts to the negative bias of zone from -1 to 0 V. The peak behavior of R_s is the result of interlayer/semiconductor interface traps under an external electric field or re-ordering and restructuring of charges at surface states or interface states at the interface. In this structure, Al₂O₃ used as an interlayer reduces the effect of chemically active dangling bonds at the surface of silicon, which eventually decreases the defects in graphene growth. Besides, passivating the surface with Al₂O₃ prevents thick native oxide formation at the interface. Therefore, the reduction of defects in graphene on top of Al₂O₃ can decrease the series resistance of the device. Thus, Al₂O₃ layer contributed to improving the carrier lifetime for Si substrate decreasing the series resistance, reducing the surface recombination, and decreasing the density of traps significantly causing a major reduction in the surface recombination.

90 kHz

100 kHz

200 kHz

300 kHz

400 kHz

8



Fig. 10 Corrected capacitance–voltage (C_c-V) plots of the structure



Fig. 11 Corrected conductance–voltage (G_c-V) plots of the structure

The measured $C_m G_m$ and values were corrected to eliminate the influence of R_s . The corrected conductance (G_c) and corrected-capacitance (C_c) values have been derived from Eq. 2 and 3 [17, 35–41].

$$C_{\rm c} = \left(\frac{(G_{\rm m}^2 + \omega^2 C_{\rm m}^2)C_{\rm m}}{(a^2 + \omega^2 C_{\rm m}^2)}\right); G_{\rm c} = \left(\frac{(G_{\rm m}^2 + \omega^2 C_{\rm m}^2)a}{(a^2 + \omega^2 C_{\rm m}^2)}\right)$$
(2)

$$a = G_{\rm m} - (G_{\rm m}^2 + \omega^2 C_{\rm m}^2)R_{\rm s}; C_{\rm i} = C_{\rm m} \left[1 + \frac{G_{\rm m}^2}{(\omega C_{\rm m})^2}\right] = \frac{\varepsilon_{\rm i}\varepsilon_0 A}{d}$$
(3)

 ε_0 is vacuum's permittivity (8.85×10⁻¹² F/m), A is device area, ε_i is the permittivity of the interfacial layer, d is a wideness of the interfacial layer ($\varepsilon_i = 9.1\varepsilon_0$ for Al₂O₃ layer). C_i describes the capacitance of the interfacial in the accumulation zone of $C_c - V$ curves. Figures 10 and 11 show the variation of corrected capacitance and conductance in the range of 10 kHz–400 kHz, respectively. As shown in Fig. 10, C_c values decrease with an increase in frequency. On the other hand, as shown in Fig. 11, G_c values increase with increasing frequency. Also, G_c –V curves indicate a peak in the negative voltage zone. The peak is attributed to the distribution of charge carriers at the Al₂O₃/p-Si interface. That is, the peak is associated with the interface traps.

To evaluate the interface states density (D_{it}) , an approach called the Hill-Coleman method [38] was used.

$$D_{\rm it} = \frac{2}{qA} \left(\frac{(G_{\rm max}/\omega)}{(G_{\rm max}/\omega C_{\rm i})^2 + (1 - C_{\rm m}/C_{\rm i})^2} \right)$$
(4)

where the maximum value of the G-V plots is G_{max} [35–41]. The obtained D_{it} values are presented in Table 1. D_{it} varies from $3.89 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ to $0.74 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and exhibits a decrease while going from low to high frequencies. These results guarantee that the interface state density that does not follow the ac signal, is dependent on frequency. The interface states density is in charge of decrease.

4 Conclusion

In this study, a nanostructure thin film of graphene is deposited onto Al₂O₃/p-Si by the CVD method. The electrical properties of the fabricated Al/Gr/Al₂O₃/p-Si structure have been investigated in detail. C-V and G-V characteristics have been analyzed in the frequency range 10 kHz-400 kHz. These measurements indicated that the values of G and Cdepend on both frequency and voltage. C and G values are also corrected by eliminating R_s effect. It is observed that D_{it} value decreases as frequency increases. All results pointed out that the interface states and series resistance have a critical impact on the electrical properties of the structure. As a conclusion, the prepared Al/Gr/Al₂O₃/p-Si structure can be utilized as an MIS or MOS device in electronic applications. This work thus submitted recommends that Gr/Al₂O₃ interlayer should be considered as a photodetector for the novel graphane-insulator-semiconductor devices.

Table 1 Frequency-dependent of the interface state density (D_{it}) for Al/Gr/Al₂O₃/p-Si diode in the frequency range of 10 kHz to 400 kHz

Frequency (kHz)	10	20	30	40	50	60	70	80	90	100	200	300	400
$D_{\rm it} (10^{13}) ({\rm cm}^{-2}{\rm eV}^{-1})$	3.89	2.75	2.23	1.98	1.77	1.63	1.51	1.47	1.40	1.38	1.07	0.93	0.74

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Compliance with ethical standards

Conflict of interest We have declared no conflict of interest.

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